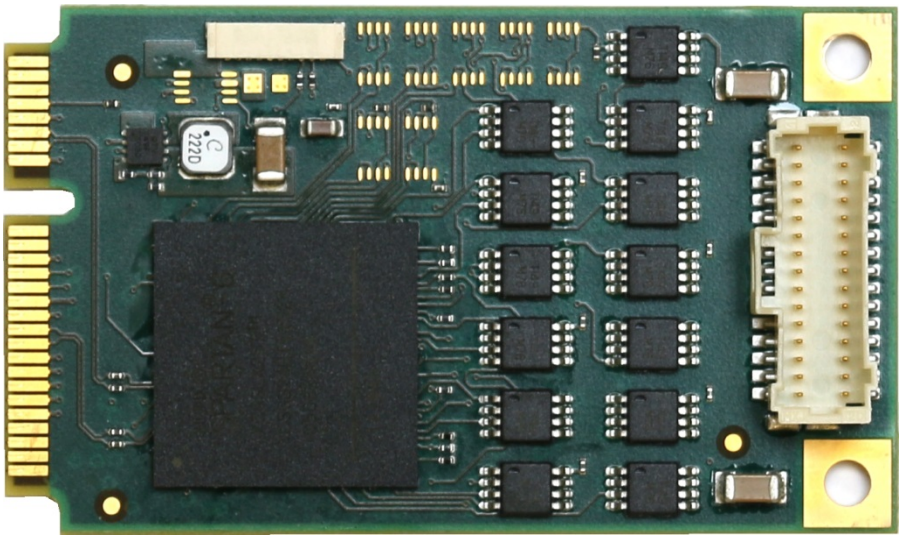
The Embedded I/O Company

TMPE633 Reconfigurable FPGA with Digital I/O PCIe Mini Card



TMPE633-12R

Application Information

The TMPE633 is a standard full PCI Express Mini Card, providing a user programmable Xilinx Spartan-6 LX25T FPGA.

The TMPE633-10R provides 26 ESD-protected 5V-tolerant TTL lines, the TMPE633-11R provides 13 differential I/O lines using EIA 422 / EIA 485 compatible, ESD-protected line transceivers and the TMPE633-12R provides 13 differential I/O lines using Multipoint-LVDS Transceiver.

All I/O lines are individually programmable as input or output. TTL I/O lines can be set to high, low, or tristate. Each TTL I/O line has a pull-resistor to a common programmable pull voltage that can be set so +3.3 V, +5 V and GND. Differential I/O lines are terminated, RS-485 lines with 120 Ω, M-LVDS lines with 100 Ω.

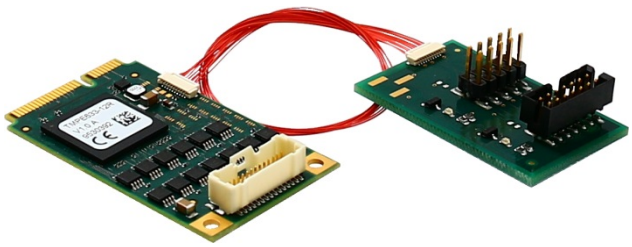
The I/O signals are accessible through a 30 pin Pico-Clasp latching connector.

The User FPGA is configured by a SPI flash. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using Xilinx “ChipScope”). For direct JTAG access to the FPGA using the Xilinx Platform Cable USB, the TA308 Programming Kit is required.

User applications for the TMPE633 with XC6SLX25T-2 FPGA can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com.

TEWS offers a well-documented basic FPGA Example Application design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TMPE633. It implements local Bus interface to local Bridge device, register mapping and basic I/O. It comes as a Xilinx ISE project with source code and as a ready-to-download bit stream.

Please note: The basic example design requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (downloadable from www.xilinx.com, a 30 day evaluation license is available).



TA308 with TMPE633-12R

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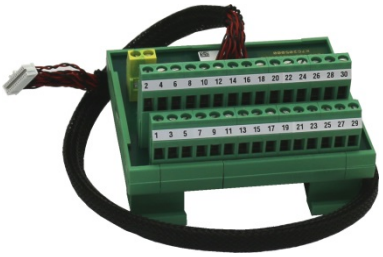
TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

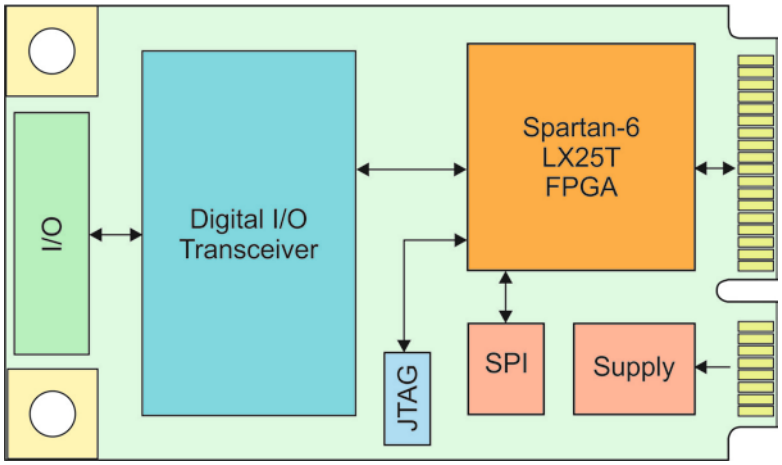
TA308 with TMPE633-12R & Platform Cable USB



TA309

Technical Information

- Form Factor: Full-Mini Card
  - Board size: 50.95 mm x 30 mm
  - PCI Express 1.1 compliant interface
- Xilinx XC6SLX25T-2 Spartan-6 User programmable FPGA
  - PCIe endpoint in FPGA
- 64 Mbit SPI-EEPROM for FPGA configuration and User Data
- Digital I/O
  - 26 ESD-protected 5 V-tolerant TTL lines with programmable pull resistor (-10R)
  - 13 differential RS-485 lines (-11R)
  - 13 differential M-LVDS lines (-12R)
  - Direction individually programmable
- I/O access
  - 30 pin Pico-Clasp latching connector
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 GB 20°C)
  TMPE633: 980.000 h



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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

Order Information

RoHS Compliant

TMPE633-10R	26 TTL I/O, Spartan-6 LX25T FPGA
TMPE633-11R	13 RS-485 I/O, Spartan-6 LX25T FPGA
TMPE633-12R	13 M-LVDS I/O, Spartan-6 LX25T FPGA

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

TMPE633-DOC	User Manual
TMPE633-FDK	FPGA Example Design

Related Products

TA308-10R	Cable Kit for Modules with XRS JTAG Connector
TA309-10R	Cable Kit for Modules with Pico-Clasp Connector

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com