

PCI Interface

All Models include an industry-standard interface fully compliant with PCI bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported.

► functionality, but processing resources up to an additional 640 DSP48E slices.

Option -104 installs the J3 connector (Model 7258) or the J2 connector (Model 7358) with 16 pairs of LVDS connections to the processing FPGA and 16 pairs to the interface FPGA for custom I/O.

With Model 7258D, the option provides an additional 16 pairs of LVDS connections through the J5 connector to the processing FPGA and 16 pairs to the interface FPGA.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SMC connector can be used to provide a 10 MHz system reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to two slave 7258D's and three slave 7358's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Two independent 256 MB banks of DDR2 SDRAM are available to the processing FPGA. These can be upgraded to 512 MB banks with option -140.

Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering and D/A waveform playback mode. All memory banks are supported with DMA engines for easily moving data through the PCI interface.

Specifications

Models 7258 or 7358: Dual version

Model 7258D: Quad version

Model 7258D shown in the Specifications

Front Panel Analog Signal Inputs (4)

Input Type: Transformer-coupled, front panel female SMC connectors

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 250 kHz to 750 MHz

A/D Converters (4)

Type: TI ADS5463

Sampling Rate: 20 MHz to 500 MHz

Resolution: 12 bits

D/A Converters (4)

Type: TI DAC5688

Input Data Rate: 250 MHz max.

Output IF: DC to 300 MHz

Output Signal: 2-channel real or

1-channel with frequency translation

Output Sampling Rate: 800 MHz max.

with interpolation

Resolution: 16 bits

Front Panel Analog Signal Outputs (4)

Output Type: Transformer-coupled,

front panel female SMC connectors

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 250 kHz to 750 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer:

Clocks Source: Selectable from on-board programmable VCXO, front panel external clock or LVPECL timing bus

Synchronization: Clocks can be locked to a front panel 5 or 10 MHz system reference

External Clocks

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms, accepts 20 to 500 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS input/output; TTL signals for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (4)

Processing FPGA: Two Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VFX100T, or XC5VLX155T

Interface FPGA: Two Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T or XC5VFX70T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs the J3 and J5 cPCI connectors with 32 pairs of LVDS connections to the processing FPGA and 32 pairs of LVDS connections to the interface FPGA for custom I/O

Environmental Specifications

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U cPCI board

Ordering Information

Model	Description
7258	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI
7258D	Quad 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI
7358	Dual 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U cPCI
Options:	
-104	FPGA I/O through cPCI J3 for 7258 or J2 for 7358; cPCI J3 and J5 for 7258D
-140	1 GB DDR2 SDRAM, Models 7258 and 7358; 2 GB DDR2 SDRAM, Model 7258D

Contact Pentek for additional available options.